Flip-Chip Technology on Organic Pin Grid Array Packages

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ABSTRACT

As microelectronic devices become more integrated with increased functionality and higher levels of performance, the complexity of packaging technology grows proportionally. Today's silicon processes have enabled microprocessor designs to achieve very high clock frequencies. As a result of the increase in feature integration, high clock frequencies, and the power supply requirements of the latest generation of microprocessors, the density of interconnects between processor chip and substrate has been increased remarkably. New package substrate technologies with enhanced interconnect density are required in order to take full advantage of these silicon advancements. This has created an array of challenges in package design, substrate technology development, and assembly processes development. To provide a highly integrated and lower cost package, the Flip Chip Pin Grid Array (FCPGA) package was proposed as an innovative packaging solution [1]. This package utilizes laser-drilled blind/buried vias stacked on a PTH to ease routing and to lower the power supply loop inductance. In addition, the integration of flip-chip technology on an organic substrate helps to provide adequate signal and power supply interconnects. The FCPGA package was designed as a socketable solution. By taking advantage of the existing PGA socket infrastructure, this package helped to expedite the Original Equipment Manufacturers (OEMs) acceptance of the new package. This paper also describes the challenges encountered in the past in package design, validation, and assembly process development. Several technical challenges such as meeting the stringent impedance requirement to enable RDRAM* bus functionality, the optimal pinning process to certify Surface Mounted Technology (SMT) pins, and Underfill material and process development to fulfill throughput and performance requirements were overcome. The FCPGA package not only delivered a package with high performance on a cost-effective substrate, but also intelligently reused existing assembly equipment to minimize overall packaging cost. With the success of the first-generation FCPGA package technology certification, which has been utilized in the Intel® Pentium® III microprocessors, future generations of this technology will be developed that should offer great advantages for future Intel products.

INTRODUCTION

The need for high-density interconnects in a cost-effective flip-chip package was the motivation for FCPGA technology development. This paper describes the challenges encountered during the first generation FCPGA package design, validation, assembly processes, and material development.

FCPGA was designed as a socketable solution. The pin side view of an FCPGA package is shown in Figure 1. The use of the existing 370 socket infrastructure helped with the OEM acceptance of this new package.

The key features of the FCPGA technology are as follows:

1. Stackup

The substrate is comprised of an FR-5 equivalent core with two resin build-up layers on each side. Both blind and buried vias are used to ease package routing.

2. Bump Pitch

The flip-chip interconnects are built on an organic substrate with a solder bump pitch of 11 mils (279.4 μm).

* Other brands and names are the property of their respective owners.

3. Decoupling Capacitors

Pin side decoupling capacitors were added to lower the power supply loop inductance.

4. Surface Mount Package Pins

SMT pins were used to ease package routing. This was an improvement over through hole mounted pins. The use of SnSb solder to join the package and pins provided solder joint reliability through subsequent reflow operations.

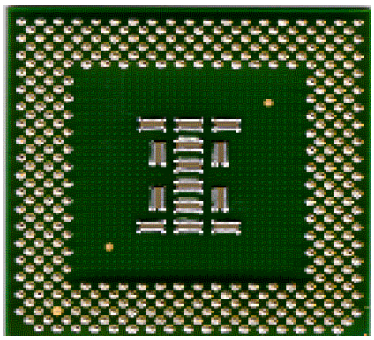

Figure 1: Pin side view of the FCPGA package

Package Design and Validation Overview

Package Designs

Several test vehicles and test structures were designed and analyzed to validate the package's electrical, thermal, mechanical, and reliability performance. Key attributes of several packages are tabulated in Table 1 [2, 3, 4, 5].

Table 1: Package design attributes

Attributes	Test Package A	Test Package B	Test Package C
Form Factor	1.95" x 1.95"	1.95" x 1.95"	1.95" x 1.95"
Thickness	1.1 +/- 0.1 mm	1.1 +/- 0.1 mm	1.1 +/- 0.1 mm
Package Layers	6 layers	6 layers	6 layers
Mn. Bump Pitch	279 µm	279 µm	279 µm
Bump Pattern	FCR in three I/O rows Square gird in core area	FCR in three I/O rows Square grid in core area	FCR in three I/O rows Slight offset parallelogram grid in core area
# of C4 bumps	1199	1286	1209
Die Size	0.355" x 0.455"	0.440" x 0.363"	0.438" x 0.386"
Die Layers	short loop	full loop	full loop
Core Voltage	>25V	1.5V / 1.6 V	1.55V / 1.8V
Package Stackup	L1/L2 : signal layers L3-L6 : plane layers	L1 : signal layers L2, L5 : partial signal layers L3, L4, L6 - plane layers	L1, L2 : signal layers L3-L6 : plane layers
Vias	Single-layer µ-vias Two-layer µ-vias	Single-layer µ-vias	Single-layer µ-vias
Footprint	PGA_370	PGA_370	PGA_370
# of chip cap.	18	14	7
Power Dissipation	>30 W	15~28 W	15~20 W

The layer structure of an FCPGA substrate is displayed in Figure 2; the targeted thickness of each layer and package key feature sizes are given in Table 2.

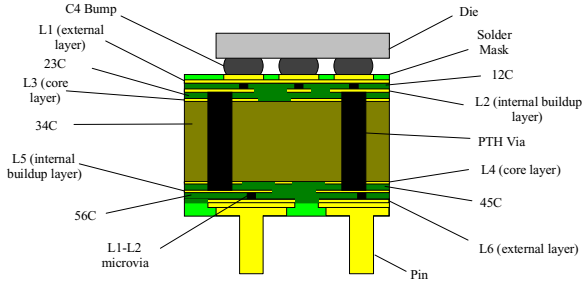

Figure 2: Cross section of FCPGA substrate

Table 2: Mean thickness of FCPGA stack up

Label	Feature	Thickness (SI)
	Solder Resist over Copper	25 µm
12C, 56C	External Buildup Layer Dielectric	30 µm
23C, 45C	Internal Buildup Layer Dielectric	30 µm
34C	Core Layer Dielectric	800 µm
L1, L6	External Buildup Layer Copper	17 µm
L2, L5	Internal Buildup Layer Copper	25 µm
	Copper over PTH	17 µm
L3, L4	Core Layer Copper	14 µm
	Total Package Thickness	1.1 mm

Electrical Characteristics

Empirical measurements and electrical modeling were used to assess the characteristic impedance (Zo), inductance, capacitance, resistance, and dielectric of the package. These parameters will impact the overall design by influencing the signal integrity, power supply droop, and routing requirements [6].

One of the resistance test structures built into the test packages is shown in Figure 3; four point probing was used for the resistance measurement. Multiple via chains and conductor sheet resistance data confirmed that the package manufacturing process was capable of meeting targeted specifications. In order to ensure impedance values satisfied the data bus requirements, dielectric constants across a wide range of frequencies were analyzed and measured. The comparison between modeled and measured values is shown in Figure 4. The empirical data is in good agreement with analytical prediction.

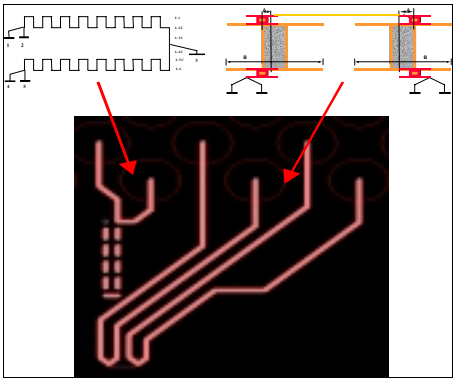

Figure 3: FCPGA resistance test structure

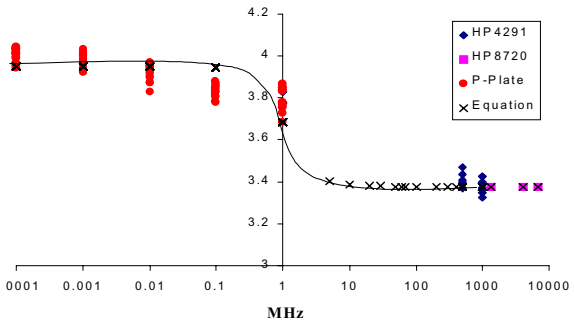

Figure 4: Comparison of calculated and measured dielectric constants in various frequency ranges

Thermal Performance

Both modeling and testing were conducted to validate the FCPGA thermal solutions. With increasing core speed and maximum power dissipation, both passive and active heat sinks were evaluated. Details of the thermal design challenges are discussed in the Thermal Designs section of this paper.

Mechanical and Package Reliability

Mechanical tests and modeling were performed to address concerns about the structural integrity of the FCPGA package. A total of 100 FCPGA samples were tested with uniform and edge-loaded forces (20 to 100 lbs). Visual inspection and post-stress electrical test data confirmed that there was no change in the mechanical and electrical integrity of the package. Moreover, an additional 40 samples were uniformly loaded up to 100 lbs. and subjected to 600 cycles of T/C "B." No sign of failures was seen, and the chip cap solder joint strength retained a healthy level as illustrated in Figure 5.

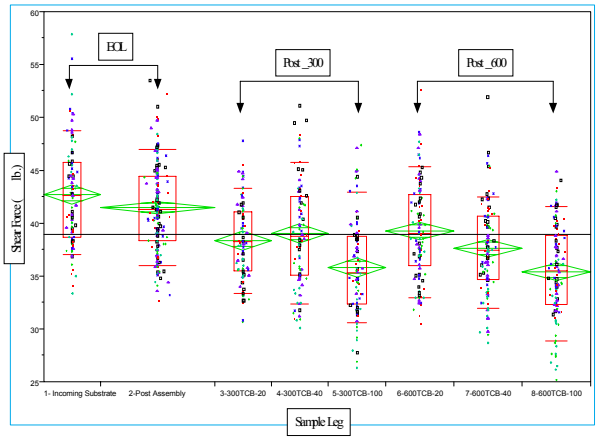

Figure 5: Chip capacitor solder joint shear strength distribution at end-of-line, 300 and 600 cycles of T/C "B"

The collected data on maximum package/die loading and chip cap solder joint shear strength confirmed the

robustness of the FCPGA package. Various stresses specified for Intel assembly technology certification (such as Temperature Cycling, Bake, Power Cycling, Shock, and Vibration, etc.) were performed to accelerate other possible failure mechanisms. Several failure modes (such as metal migration and weak pin solder joint) were observed early on, but fixes were quickly implemented, which eliminated these issues. In conclusion, there were no high-risk issues that appeared during testing that impacted the technology certification.

Continuous data was collected at Intel and at supplier manufacturing sites. This included electrical, mechanical, and thermal measurements. These data, collected since early in the development phase, built sufficient confidence that the FCPGA package was a viable packaging solution for current as well as future microprocessors.

SUBSTRATE DEVELOPMENT OVERVIEW

Photolithography and etch have been the most prevalent methods to create blind µ-vias in high-density substrates. The photolithography process has two main disadvantages. First there is the limitation to the µ-via diameter due to the limited resolution of commercial photosensitive materials. Second, photosensitive materials are prone to reliability issues with their mechanical properties, moisture absorption, and the value of the dielectric constant. Laser µ-via drilled into an "off the shelf" dielectric can overcome these limitations.

Laser technology can potentially create via sizes down to the < 10 µm range, while today's photolithography materials are limited to 50-60 µm vias. Another plus is that the smaller the via size, the lower the cost of the laser µ-via formation due to a shorter pulse time. In addition, by eliminating photosensitive resins, a large number of non-photo sensitive materials can be considered for dielectric material. The laminate material used in FCPGA is a commercially available film, which is lower in cost when compared to the dielectric materials used in other photo µ-via based packages.

In the FCPGA package, the laser drill via technology was implemented in spite of the fact that the line/space design rules were not as challenging as the existing Organic Land Grid Array (OLGA) technology. The rationale was to save money on processing costs, while taking advantage of the higher routing density resulting from the smaller µ-via pads. By using laser vias instead of photo vias, the FCPGA package had access to cheaper and better commercially available dielectric materials. Figure 6 shows a schematic of the laminates and materials used in the FCPGA.

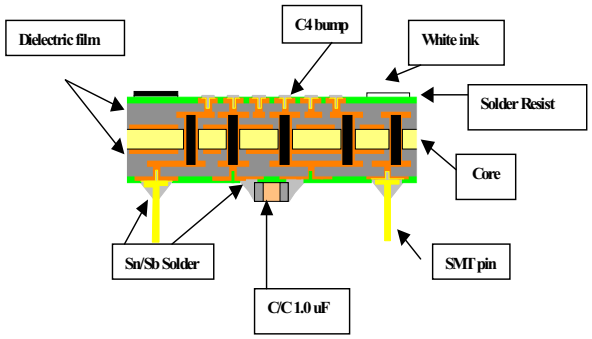

Figure 6: Schematic of FCPGA laminates and materials

Comparing FCPGA with the previous OLGA package, there are several distinct differences:

1. FCPGA uses laser vias instead of photo vias, and SMT pins.
2. The size of the FCPGA package is larger with additional area for chip caps.
3. Commercially available dielectric and solder-resist materials are used in the FCPGA package.
4. µ-via is used on PTH in the FCPGA package.

FCPGA KEY CHALLENGES

Thermal Designs

Thermal design solutions for the FCPGA package pose challenges because of the system chassis spatial constraints and the need to meet maximum power dissipation requirements. The design was also challenging because a heat sink ground feature that suppresses potential electromagnetic emission had to be integrated into the package. The key thermal design constraints are listed in Table 3. To broaden the variety of possible FCPGA package applications, both passive and active heat sink designs were evaluated. A schematic of passive and active heat sink solutions is shown in Figures 7 and 8. Preliminary empirical and modeling results suggested that passive and active solutions could support power of about 19W and 22W, respectively.

Table 3: Summary of typical FCPGA thermal design attributes

Attributes	Product A	Product B
Thermal Design Target	19.3 W	22 W
Tj	90 oC	85 oC
Ta (system internal)	45 oC	45 oC
Theta_ja	2.33 oC/W	1.59 oC/W
Airflow = 200 fpm	200 fpm	150 fpm
Clip force requirement	12 - 20 lb	12 - 20 lb
HS design	passive	active
HS weight	140 - 180 g	140 g

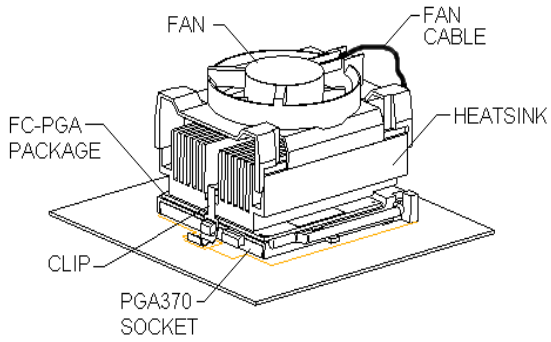

Figure 7: Schematic of an active heat sink solution

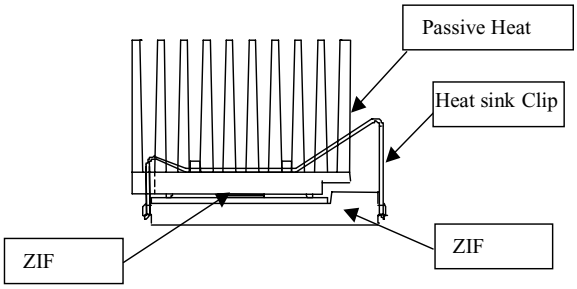

Figure 8: Schematic of a passive heat sink solution

High-Speed Bus Impedance Requirement

High-speed digital systems have problems that manifest themselves in three distinctive ways. First, conductor traces can experience reflections due to multiple impedance mismatches. Second, cross talk may occur because of unwanted electromagnetic coupling between adjacent traces. Third, ground bounce can be significant due to inductance in the ground return path of the IC package. The combined result of these effects could adversely impact timing margins in systems and thus limit the ultimate performance of the system. In the FCPGA package, a good deal of effort was put into controlling the impedance to limit the impact of the first problem.

The design of a fixed-impedance bus structure makes it more sensitive to the physical dimension tolerances in the manufacture of the package. The FCPGA design rules will support multiple impedance targets in the package. The bus impedance specifications call for a tolerance target of +/- 10%.

Impedance is a function of dielectric layer thickness, dielectric constant, and Cu trace width. This requires rigorous tolerance control of dielectric thickness. Non-uniformity in thickness of the Cu plating will directly add variability to the thickness of the dielectric layer between two adjacent Cu layers. Since there is inherent Cu thickness variation, the control of dielectric layer thickness variation becomes even more stringent.

Initial data indicated this variation would be a challenge for the FCPGA package as there was a higher dielectric thickness variance than desired, and a correspondingly variable impedance value. However, as illustrated in Figure 9, impedance (Zo) measurements taken after process improvements showed that the mean impedance stabilized. The improvement was made possible through improving the Cu thickness uniformity and by making a smoother insulator surface.

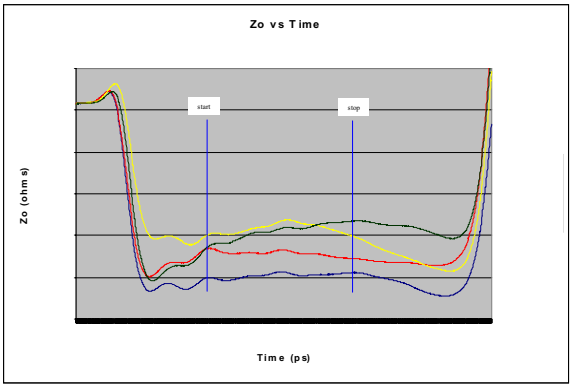

Figure 9: Impedance measurements with two different dielectric thicknesses

µ-Via Reliability Issues

Preliminary reliability data showed µ-via delamination. The µ-via delamination resulted in a high-percentage fall-off after 300 cycles of T/C "B" (-55C <-> 125C) stressing and higher cumulative fails after 1000 cycles of T/C "B". Figure 10 shows an example of a delaminated via that caused an electrical failure.

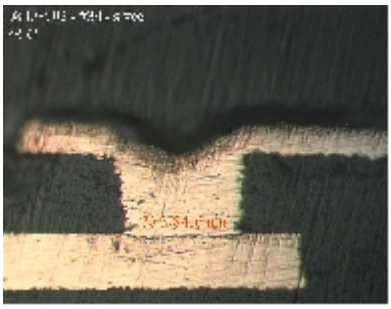

Figure 10: Example of a delaminated via

Failure analysis suggested that via delamination occurred at the interface between the electrolytic Cu and electroless Cu layers. Hot oil thermal shock tests were utilized as a quick-turn reliability monitor. The measurement of improvements in the manufacturing process were based on the shifts in the µ-via resistance. Test data confirmed that two factors were the significant modulators in µ-via delamination. Figure 11 shows a schematic drawing of various via structures, as well as the test data for µ-via resistance shift after hot oil thermal shock. The test results clearly indicated that via resistance increased more than 50% after thermal shock for some test structures. After process fixes were implemented, no via resistance shift was seen after 400 cycles of stress!

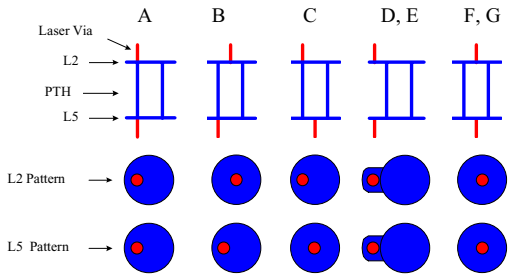

Figure 11a: Schematic of various via structures

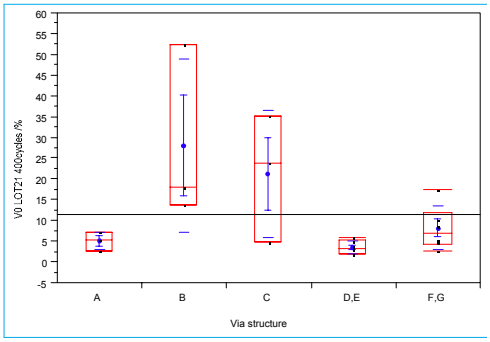

Figure 11b: Via resistance before process fix

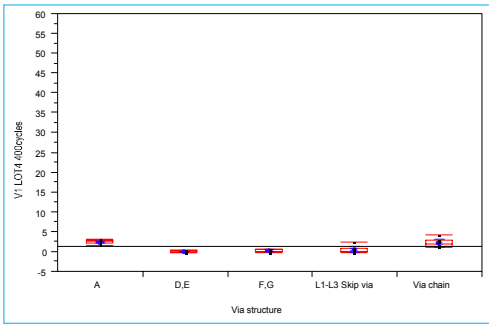

Figure 11c: Via resistance after process fix

The improvement in via integrity was also verified through via "pop" tests. Three types of failure modes were observed and are shown in Figure 12. None of these failure modes appeared on FCPGA packages after the process fixes were implemented.

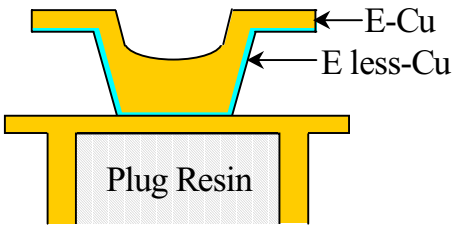

Figure 12a: Schematic of a PTH via structure

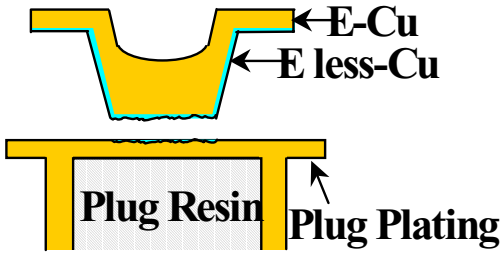

Figure 12b: Popped via failure indicating weak bonding at the two Cu layers interface on package before process fix

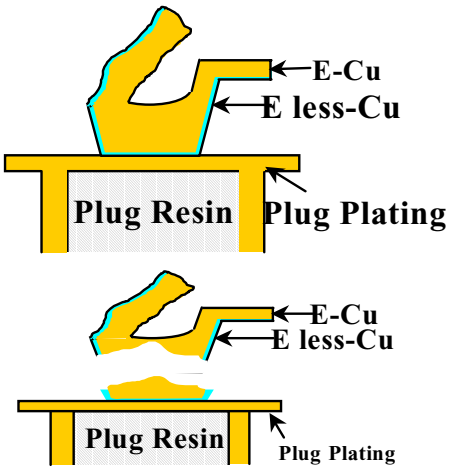

Figure 12c: Broken via edge indicating strong Cu layer interface on package after process fix

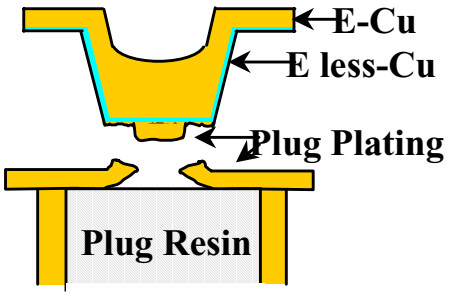

Figure 12d: Broken via plug plating indicating strong bonding at the two Cu layers interface after process fix

SMT Pin Development

The FCPGA package utilizes SMT butt-mounted pins on an organic substrate. To determine the reliability of these pins, experiments were conducted to evaluate different combinations of pin solder joint structures. They were made from three solder materials, three different solder volumes, skew misalign pins, and smaller pin nail-head sizes. The attributes of each leg of the experiment are detailed in Table 4. Additionally, pin pull and pin shear testing were used to quantify the pin strength before and after stresses.

Table 4 : SMT pin strength attributes

Legs	Nail Head Diameter (mm)	Solder Volume (mg)	Solder Composition	Pad Opening (mm)
A	0.9	M	SnAg	1.2
B	0.7	H	SnAg	1.2
C	0.9	H	SnAg	1.2
D	0.9	M	SnAg	1.2
E	0.9	L	SnAg	1.2
F	0.9	H	SnSb (A%)	1.3
G	0.9	H	SnSb (A%)	1.2
H	0.9	M	SnSb (A%)	1.2
I	0.9	H	SnSb (B%)	1.3
J	0.9	H	SnSb (B%)	1.2
K	0.9	M	SnSb (B%)	1.2

Test data confirmed that the smaller pin nail heads and intentional pin misalignment had lower pin strength as measured before assembly. Legs with M mg and H mg of SnAg and SnSb legs showed comparable pin pull strength and pin shear strength with the exception of the L mg SnAg lot, which had lower pin pull and pin shear strength. Interestingly, after assembly, the SnAg lots' pin pull strength was reduced significantly. Both SnSb (A%) and SnSb (B%) lots showed no sign of pin joint strength degradation after assembly. The SnSb (B%) was selected as the POR material because SnSb (A%) required a higher reflow temperature, which was undesirable.

Low Cost Underfill Material and Process Development [7]

The use of a two-step process and two separate materials for Underfill and fillet in C4-OLGA packages resulted in high equipment costs and a narrow process window. The challenge in FCPGA was to develop a low-cost, but high-performance Underfill material that would enable a simplified process and deliver high yields and improved unit per hour (UPH) capability.

Underfill material selection criteria included raw material cost, manufacturability, reliability and process integration performance, and supplier technical support and quality. The Underfill development team also reexamined the reliability and manufacturability success criteria such as alpha particle counts and the number of voids and voiding sizes, used in previous stages of development.

In developing the new Underfill process, viscosity and self-fillet formation are two key epoxy material properties. Based on material data sheets provided from fourteen suppliers worldwide, a total of four different materials was chosen for further evaluation. Score cards from each of the candidates were assessed to collect technical, business support, and quality data. Based on the collected information, the POR Underfill material was then selected. After the POR material was finalized, the

epoxy module engineering team focused on Underfill process optimization. Collaborative effort from the development team resulted in an optimized and simplified Underfill flow that met the FCPGA cost targets.

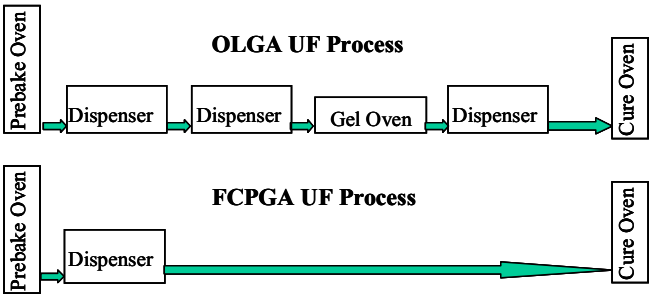

Figure 13: A comparison of the C4-OLGA and the FCPGA Underfill processes

Figure 13 illustrates the differences between the C4-OLGA and the FCPGA Underfill process flows. As shown in the POR flows, the FCPGA process has one, instead of two, dispensers and a BTU, which could save on equipment expenditures. Moreover, when results were evaluated, the FCPGA also improved the yield, and it had higher UPH throughput. The simplified Underfill process, together with the high performance of the Underfill material, was a plus for the FCPGA program.

Flip-Chip Solder Bump Non-Wet

Initial FCPGA data collection indicated the highest pareto of yield loss was attributed to open failures due to the non-wet of the C4 bumps. Low yield analysis revealed that the non-wet falls into two categories:

- edge non-wet, raccoon tail type, which can be detected with X-ray
- center non-wet, which is invisible with X-ray

However, in the second-phase data collection, a new oven was used for FCPGA reflow, and the open failures due to non-wet were reduced significantly. Low yield analysis confirmed the majority of non-wets were at the center of the die and invisible with X-ray.

A root cause assessment of the center non-wet showed no correlation between the microprocessor chip's passivation oxide thickness or co-planarity, the substrate's bump oxide, flux quantity, or uniformity during the chip attach process. A cross section of the center non-wet unit's solder bump joints revealed the substrate's and chips' bumps were not adequately aligned, except for those at the middle of the die. The right and left sides of the bump joints were slightly misaligned at opposite directions. Because of these observations, a failure mechanism for center non-wet was proposed; as illustrated in Figure 14, it turned out that the lack of bump co-planarity in the substrate prevented solder joints from forming at the center region of the die. This model also explained the slight shift in the alignment of the substrate's and die's bumps near the edge of the die.

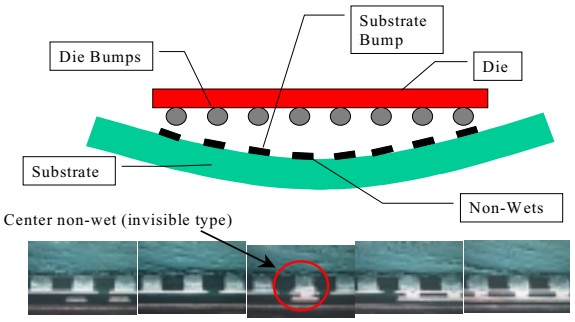

Figure 14: Proposed center non-wet mechanism; excessive substrate bump co-planarity prevents solder joints from forming at the center area of the die

The proposed model was validated through experimentation. From the data, we also realized that a maximum substrate bump co-planarity was required to prevent center non-wet. This has been defined in the specification for incoming packages.

FUTURE DEVELOPMENTS

The next generation of FCPGA package design rules have been defined and are currently under development. The performance enhancements in the new FCPGA2 package will be achieved with finer feature sizes (including bump pitches, Cu trace width and spacing, PTH size, stripline, etc.) and the addition of some new features (such as stacked vias and via-in-via). In addition, power delivery and removal capabilities will be improved through better decoupling capacitance and the use of a highly conductive package lid.

CONCLUSION

The FCPGA package design and development efforts have resulted in the integration of high-density flip-chip interconnect, SMT pins on an organic substrate. This new package is also high yielding, manufacturable, reliable, and low in cost. This cost-effective packaging technology represents a shift in direction from the previous OLGA technology, and it also represents a significant milestone in the evolution of organic substrate technology.

ACKNOWLEDGMENTS

The design and development of the FCPGA is a joint effort that spans several different organizations. We thank the entire FCPGA package design team, substrate development team, ATTD/QRE, and the assembly processes development staff for their hard work and devotion to support the development of this technology. We also acknowledge the great help received from the ATTD, ATTD/QRE/FA, and ATMO/CSMO divisions and other organizations. Finally, our special thanks to N. Grayeli, D. White, Jeff Watson, and M. Tay for their guidance and encouragement during packaging development. Finally, our thanks to the many others who contributed to the development of this program.

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